

Digitization at the Feed Through: Circuit Design

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## ABSTRACT

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A major challenge in modern particle physics experiments is to reduce and control the noise or background signal of the experiment. These unwanted signals could affect the experiment's performance and cause many problems in the future analysis of data. The MicroBooNE detector is a liquid argon time projection chamber for detecting neutrinos. One of the concerns with the MicroBooNE detector is the contamination of analog signals from noise that is introduced either through the process of digitization or by a long cable run to the data acquisition system. A redesign of the feed through electronics can help reduce the contaminating noise by digitizing the signal with a Wilkinson digital converter immediately after the feed through of the detector and by allowing a longer cable run. Many changes have been made to the schematic and layout of the control card that houses the pulse shapers, time-to-digital converters, and Ethernet port. Many options for designs and components have been included on the new board so that they can undergo ample testing before final decisions are made. The eventual goal is to have a design for a control card that implements a low-noise digitization process, can reside immediately after the detector feed through, allows for a longer cable run, and fits in the same dimensions as the previous board.

## INTRODUCTION

MicroBooNE is a liquid-argon (LAr) time projection chamber (TPC) detector. The TPC operates by having a voltage difference across the detector. As a charged particle passes through the detector, it can ionize the argon, and the electric field from the voltage difference causes the free electrons to drift towards three planes of wires. The planes of wires include two induction planes and one collection plane [1]. The drifting electrons induce a current on the first two planes as they pass through and are then collected on the third plane. These currents, along with timing information from 30 photomultiplier tubes, can be used to reconstruct the passing particle's track in the detector. Few liquid-argon TPCs have been constructed as R&D for future detectors — ArgoNeuT being the latest with an active volume of 0.0003 kton. MicroBooNE will have an active volume of 0.1 kton, being the largest detector of its kind [1]. It will serve as both research and development for future detectors possibly including the Long-Baseline Neutrino Experiment (LBNE), and as an opportunity to explore the physics of low-energy neutrino interactions [2].

Once the analog signal has been produced, it must be sent out of the detector, digitized and sent to the data acquisition system (DAQ). The main concerns with the technical process of collecting the data are reliability, noise, and appropriateness of the design specs [3]. The option of digitizing immediately after the analog signal leaves the detector is desirable because it can

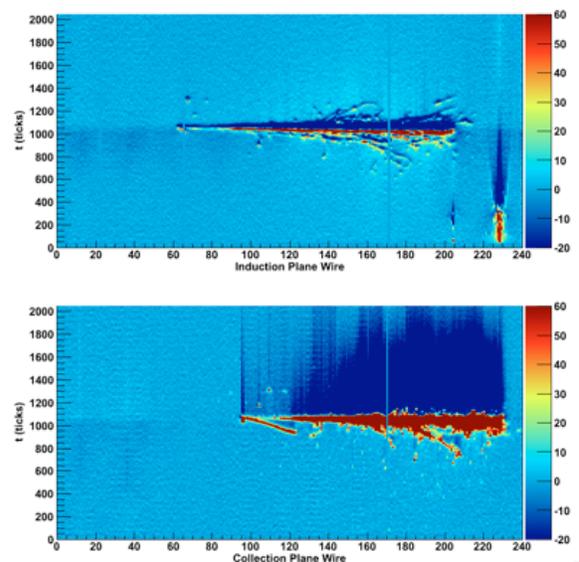


Figure 1: TPC tracks of an electron neutrino interaction candidate from ArgoNeuT, showing tracks from both the collection and induction planes.

help improve noise performance and allow for a longer cable run to the DAQ. The concerns with this option include power consumption and cooling concerns as well as difficulties of servicing the electronics [2]. The goals with using feed through electronics are to digitize the analog signal before they are contaminated by noise and to minimize the number of digital activities in the digitization process [3]. The process of digitization used currently is known as a Wilkinson analog-to-digital converter (ADC). In this process the analog signal is compared with a known reference voltage. By sending both of these signals through a comparator, the return is digital pulses whose length corresponds to time samples. By knowing the time samples and the

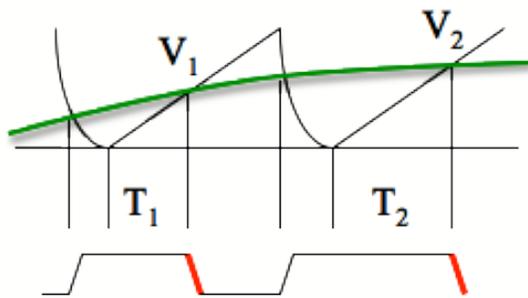


Figure 2: Time and voltage samples with a reference voltage (black) and analog signal (green).

reference voltage, the original analog signal can be reproduced. For MicroBooNE, the ADC sample rate needs to be around 2 MHz with an ADC resolution of about 12 bits [2]. These requirements are already implemented in the current design for the digitizer and must be considered for the changes made to the design.

## MATERIALS AND METHODS

### *Current TPC Readout Board Design*

The current design for the TPC readout board includes a pulse shaper that leads to an ADC. Once the ADC has digitized the analog signal, it passes it on to a field programmable gate array (FPGA) [2]. The FPGA works with onboard memory before sending the data to the DAQ PCs through an optical link. After the feed through, the cable run is housed in a Faraday cage to reduce noise that could contaminate the signal. The design for the cable driver, pulse shaper, and ADC driver includes three differential operational amplifiers to prepare the analog signal before

getting to the ADC. There must be one of each of these circuits for each channel from the detector [3].

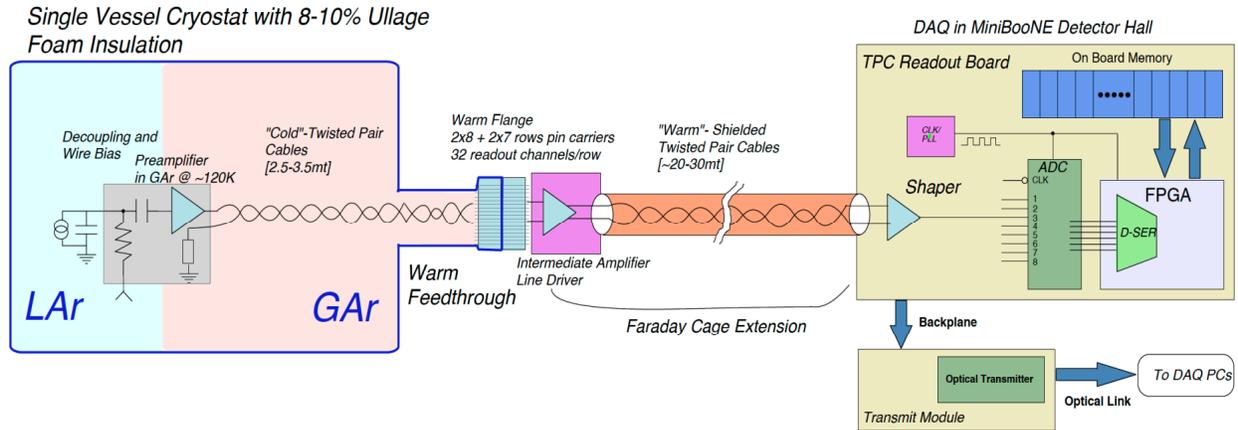


Figure 3: Diagram of the electronics from the detector to the DAQ for MicroBooNE, including the cold electronics before the feed through, the feed through electronics, the cable run and the TPC readout board.

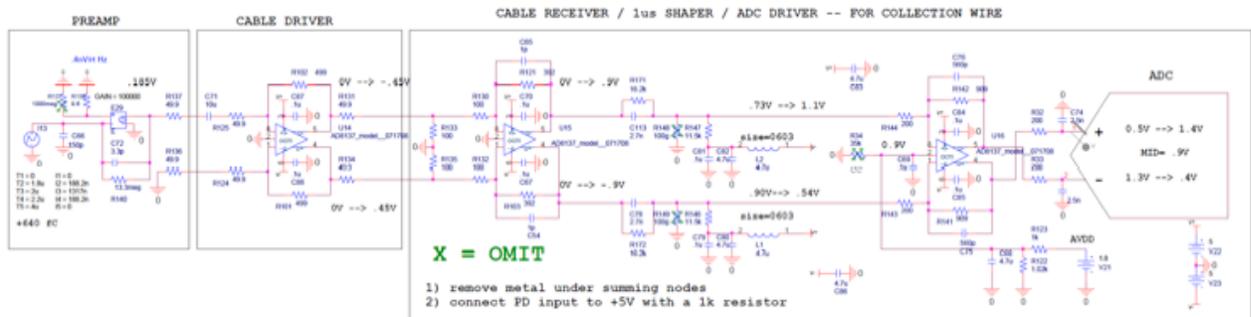


Figure 4: The schematic for the electronics that prepare the analog signal for the ADC, including the pulse shaper.

### Fast TDC Control Card

In an attempt to reduce the noise in the digitization process and allow for a longer cable

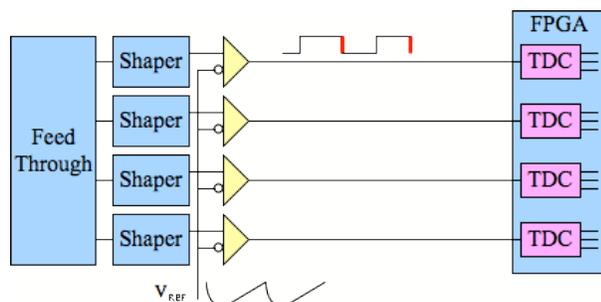


Figure 5: Diagram of the Wilkinson ADC with the pulse shaper, followed by a comparator and then an FPGA with TDCs.

run a fast TDC control card can be used instead of the current TPC readout board [3]. The fast TDC control card replaces the ADC with the Wilkinson ADC by using a comparator to compare the analog signal and the reference

voltage and a time-to-digital converter (TDC) to change the time samples into voltage samples of the analog signal. The current TDC control card has multiple FPGAs. One FPGA has the same responsibilities as the FPGA in the TPC readout board; it handles the data with the memory and sends it to the DAQ PCs [2]. The other FPGAs are necessary for housing the TDCs. Depending on the ability of the FPGA, a different number of these may be necessary. The switch from an ADC to a TDC has been tested for reassurance that the TDC has the necessary sample rate and resolution [3].

### ***Redesigning the Fast TDC Control Card***

Before working on changes to the schematic and layout of the fast TDC control card, it was necessary to take into careful consideration the size of the board and the options that were to be included for testing. There are two main comparator/TDC options that are to be included in this design of the board that will influence the decision of components and design [3]. Option 1: The pulse shaper and reference voltage will feed directly into a separate comparator, which will then send the time samples into an FPGA that houses the TDC. Option 2: The pulse shaper and reference voltage will feed into an FPGA that houses both the comparator and TDC. The decision of which option to use depends on cost of the comparator components and the performance of the comparator implemented on the FPGA. The new design will use both of these options for different analog input channels so that they can undergo testing. In regards to the board size, the current design for the pulse shaper is too large to fit on the preferred board size of 5.2" x 2.25" [2]. This requires changes made to the design so that it can fit comfortably. There are also considerations of using a new FPGA that can handle more input channels and a new implementation of the Ethernet controller that reduces the number of components necessary [3]. Both of those changes will save space on the fast TDC control card.

## RESULTS

### *Pulse Shaper*

The old design for the pulse shaper was a three-stage amplifier that prepared the analog signal before being digitized. In an effort to reduce the layout size of the circuit, two of the operational amplifiers were combined making the new circuit a two-stage amplifier. In combining the two operational amplifiers, the overall gain of the pulse shaper remained the same; it also allowed the removal of many other components such as certain bypass filters that helped with reducing the size. Half of the pulse shapers were implemented with comparators for the testing of Option 1, while the other half will send the signal directly to an FPGA for the testing of Option 2.

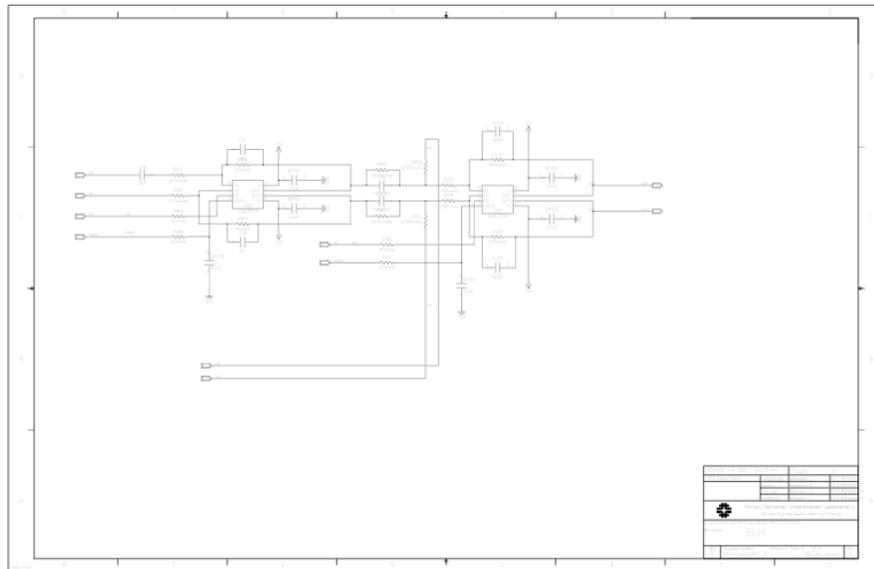


Figure 6: The new schematic for the pulse shaper without a comparator; this design requires the comparator to be implemented on the same FPGA as the TDC.

### *Ethernet Controller*

The previous Ethernet controller design used two separate chips; an Internet connectivity chip for providing the TCP/IP addresses and a PHYceiver chip for handling the communication to the Ethernet port. A new single chip, the WIZnet Ethernet W5100, acts as a TCP/IP stack with

PHYceiver capabilities, allowing the replacement of both chips. The new Ethernet controller design saves space while preserving the functionality and performance of the old design.

### ***FPGA***

The current FPGA in use to house the TDC can only handle 16 input channels per FPGA. The fast TDC control card is planned to have 32 analog input channels. Two FPGAs will be required to handle all the input channels. Other FPGAs being considered include the Cyclone III EP3C40 that will be able to handle all of the input channels on a single FPGA. The Cyclone III EPC40 is also being implemented on the new board design for future test.

### **DISCUSSION/CONCLUSION**

The new design of the fast TDC control card will present a valuable option for low-noise digitization at the feed through. The Wilkinson ADC implemented with a TDC satisfies the requirements of MicroBooNE's digitizer and can be used in a number of designs that will reduce the contaminating noise on the analog signal. With the new pulse shaper design, 32 pulse shapers can comfortably fit on the current board size. Sixteen will reside on each side and it will require two of the current FPGAs to house the TDCs. Both options for the placement of the comparator will work as a Wilkinson ADC, but more tests are necessary to determine the performance of the FPGA comparator. The new board's overall design is intended to include many options that need to be tested and it will include both comparator options, a new Ethernet controller and a new single FPGA for handling all 32 input channels.

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