

Abstract

The MicroBooNE detector project is set to benefit from a subtle change in its digitization design. Digitization can be implemented at feed through instead of over 20 meters away from the signal source. We have a designed card with capability of digitizing signals at feed through. The card has added features which include a high time resolution (up to 50ps LSB) and an efficient noise handling. The card is compatible with the detectors; the card is designed to fit the slots available at feed through. The digitization scheme used is a TDC implemented on an FPGA. Dedicated carry lines of an FPGA are used as delay cells to perform time interpolation within the system clock period and to realize the fine time measurement. Two Gray-code counters, working on in-phase and out-of-phase system clocks respectively, are designed to get the stable value of the coarse time measurement. The fine time code and the coarse time counter value, along with the channel identifier, are then written into a first-in first-out (FIFO) buffer. Tests have been done to verify the performance of the TDC. This paper explains the TDC card design and the details the performance test carried on the card.