

A Demonstration of Digital Control of the VTS RF system

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Abstract

A brief overview of the designed Phase-Locked loop (PLL) digital control is presented. Its performance is compared with that of current analog PLL in the Low-Level Radio Frequency control (LLRF) of Vertical Test Stand (VTS). Data of noise transmitted power and cavity pressure are also presented.

Introduction

Fast-working boards based on Field-Programmable Gate Array chips (FPGA) are widely used for problems, requiring fast feedback loops. Particularly, they are increasingly being used for controlling microphonics and Lorence force detuning control of superconducting cavities, when a fast and precise driving signal for piezo actuator is needed to be generated. There is, however, a limited usage of FPGA boards for Low-Level Radio Frequency (LLRF) control. Instead, expensive and sophisticated in control analog circuits are applied there.

In this paper we aimed to demonstrate a viability of using FPGA circuits instead of commonly used analog components. In that particular case the original analog Phase-Locked loop (at VTS LRRF) was substituted with one, implemented on FPGA board: we designed a digital phase detector, and conducted a set of tests on VTS LLRF, comparing that with the original one. The results appeared to be comparable, and in some cases digital board behaved even better.

Methods

Any LLRF cavity control requires signal processing of a probe, forward and reflected IF signal, coming from the cavity.

In our work we performed this processing by using Nallatech Virtex-4 board that is based on FPGA chip, clocked at 100 MHz (It does, however support external clock option) The chip contains re-programmable logic components and interconnects. These components can be used to perform basic logical functions as

well as complex numerical processes. The board also has 2 independent sets of 14-bit ADC and DAC channels, working at a speed of 105 MSPS and 160 MSPS respectively.

The synthesis and verification of FPGA firmware on this board is implemented with VHSIC Hardware Description Language, briefly referred to as VHDL. The board also supports C-callable libraries, so communication with the board may be performed by means of compiled Labview dynamic-link libraries (.dll) or Matlab wrappers files (.mex). In our case we used Matlab mex wrappers and wrote Matlab scripts to control the circuit by reading/writing information from the registers in the board. This made the system more flexible and not hard-wired.

Remarkably, most of signal processing that is necessary for LLRF control can be done by using just 3 basic components: NCO with adjustable frequency, Mixer, and Filter. These VHDL components were written and tested on the FPGA board, and their description is represented below

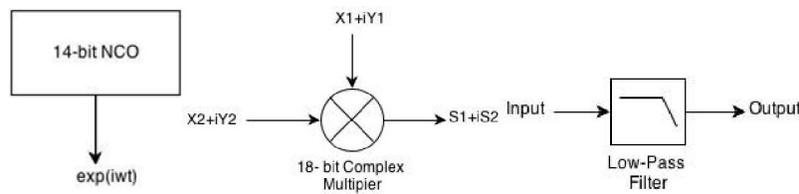


Figure 1. Basic signal processing components

- a) Complex multiplication component
- b) Numerically Controlled Oscillator component
- c) Filter component

Numerically Controlled Oscillator (NCO)

NCO component (Fig.1a) creates cosine and sine signals with 14 bit precision at a clock speed. The algorithm is based on counter-driven lookup table. 32 bit phase counter gives it a frequency resolution of 240 mHz. It also supports AM and FM modulation of the signal.

Mixer

Mixer (Fig.1b) simply performs a multiplication of two complex 18-bit signals each clock cycle, and results in 18 bit I and Q output. This component serves to down-convert or up-convert the frequency of incoming signal.

$$M = (X_1 - iY_1) * (X_2 + iY_2)$$

Filter

The last component is filter (Fig.1c). It performs the following numerical process:

$$x_{k+1} = u - x_k * \frac{dt}{\tau}$$

Here u – input signal, x_k - 32 bit accumulator, dt is a clock period and τ is the time constant of the filter. By changing τ from the registers, cut-off frequency can be changed. This can be used when the resonance frequency of the cavity is not known precisely. The filter has also a controllable gain, which is based on selecting bits in the accumulator.

Phase difference meter

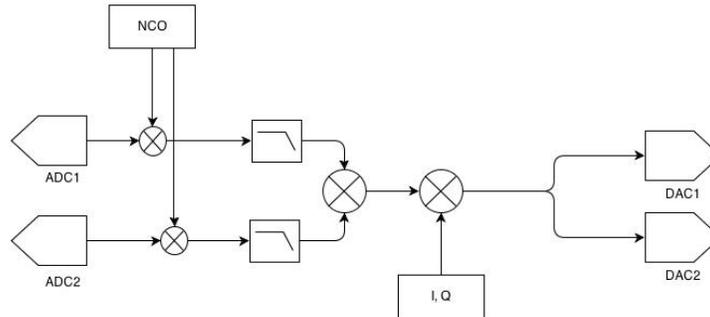


Figure 2. Digital phase difference meter

These three basic components can be assembled to a digital phase difference meter. Its block diagram is shown on the figure 4. Firstly, two of the incoming into ADC1 and ADC2 signals are down-converted by being multiplied by NCO generator signal of a similar frequency. Afterwards, to cut out higher frequencies harmonics, they are passed through low-cut filters. Finally, the first signal is multiplied by the complex conjugate of a second one, which results in the signal, proportional to the phase difference. Additionally, to adjust the phase magnitude the resulting signal may be multiplied by a constant (controlled from the register)

The NCO was attuned to work at exactly 13 MHz (this is limited by the accuracy of the crystal oscillator in the board which is usually about 50ppm i.e ~600 Hz for 13 Mhz signal). The cut-off frequency of the filters was adjusted to 10 kHz value. So these settings allowed phase meter to effectively process incoming signals of 13.00+/-0.01 MHz

LLRF simplified scheme

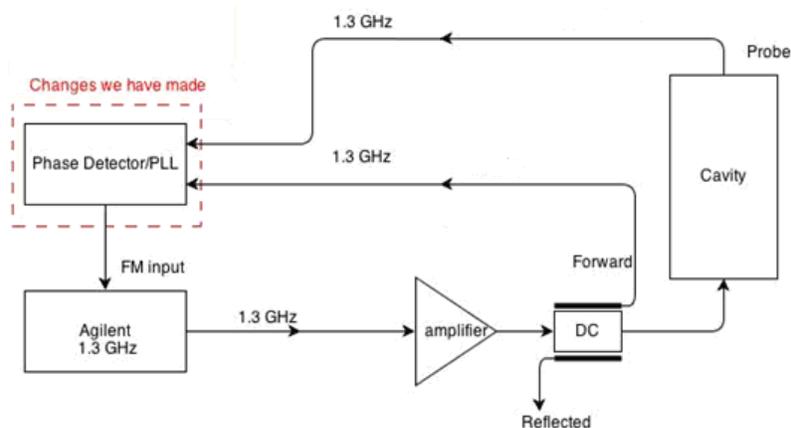


Figure 3. Simplified LLRF scheme (1.3 Ghz cavity case)

The tests were conducted on LLRF VTS facility at IB1 Technical Division, Fermilab. At the moment of the experiment 1.3GHz 9-cell TESLA-style cavity was tested there (tb9aes011).

The simplified version of how the LLRF is implemented is represented on fig.3.

(The actual complete LLRF schematics can be found online)

The 1.3 GHz reference signal of Agilent generator is firstly amplified. Then it goes through a directional coupler, and passes to the cavity. Directional coupler returns forward and reflected signals. Having gone through the cavity, the transmitted signal is mixed with the forward signal. This gives a phase difference, which then feeds to the FM input of Agilent. So every time the cavity goes off resonance, there is a nonzero phase difference signal created, that adjusts the frequency of the reference 1.3 GHz source so that to return back to resonance.

The test were run with the following settings: incident power $P_{inc} = 16W$, Reflected power $P_{ref} = 11W$, losses $P_{loss} = 5W$, quality factor $Q=3e8$, gradient $E=1.28MV/m$

VTS was connected to helium recovery line (4.5K) with “natural” pressure fluctuations at around 880 torr (quiet evening - no other experiments are running).

Our PLL's NCO works at the frequency of 13 MHz. So, in order to be able to process 1.3 GHz probe, and forward signal, these signals were down-converted to 13 MHz with a transceiver, supplied by the Accelerator Division LLRF group (AD/LLRF)

To not induce any disturbances on the ongoing tests, we substituted only the PLL part of the LLRF: the analog PLL component was substituted with our phase difference detector (Fig.3, highlighted in red color). Before doing that the digital PLL was attuned so that to have the same gain and magnitude of the phase difference, as it was in the original PLL.

After being tuned, the original PLL was unplugged from the FM input of reference signal (Agilis), and digital board was connected instead. (Appendix)

Results

Initially phase difference levels for analog and digital PLL were attuned to have the same gain and response. Their levels changed in the same every time when the cavity went off resonance,. However, one difference was that there was a 1 kHz modulation of the digital signal present. In contrast, analog signal was flat. Although we tried to change the cut-off frequencies of the filter components (inside of the digital PLL), the fluctuations neither disappeared nor changed.

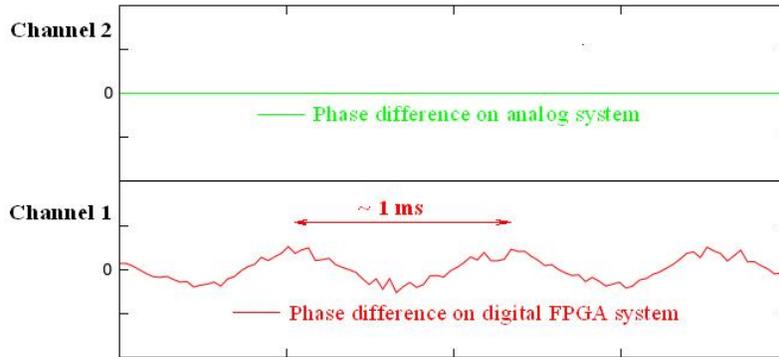


Figure 4. A sketch of the indications on the scope for the digital and analog circuits
(present for both types of cavities)

To compare the performance of both circuits we tracked the transmitted power of the cavity, and pressure variations in the Dewar vessel for a 10 minutes period. Afterwards, the relative deviations of these signals were compared (Fig.5) As one may observe, LLRF with digital phase control behaved better, than analog one, with less fluctuations in transmitted power signal present.

The absolute RMS error for pressure and transmitted power was similar (~ 0.0035 V). However, the average output values were ~ 9 V for the pressure, and ~ 1 V for the transmitted power, so the relative error was higher for the case of the pressure. The noise did not look correlated in that case.

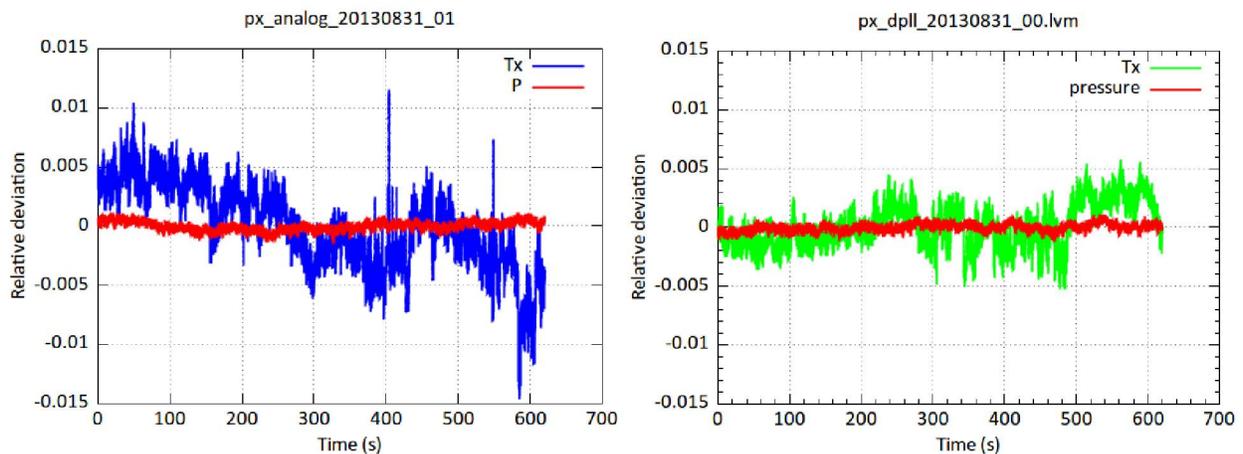


Figure 5. Tracking noise of pressure and transmitted power
digital PLL (a), original analog PLL (b)

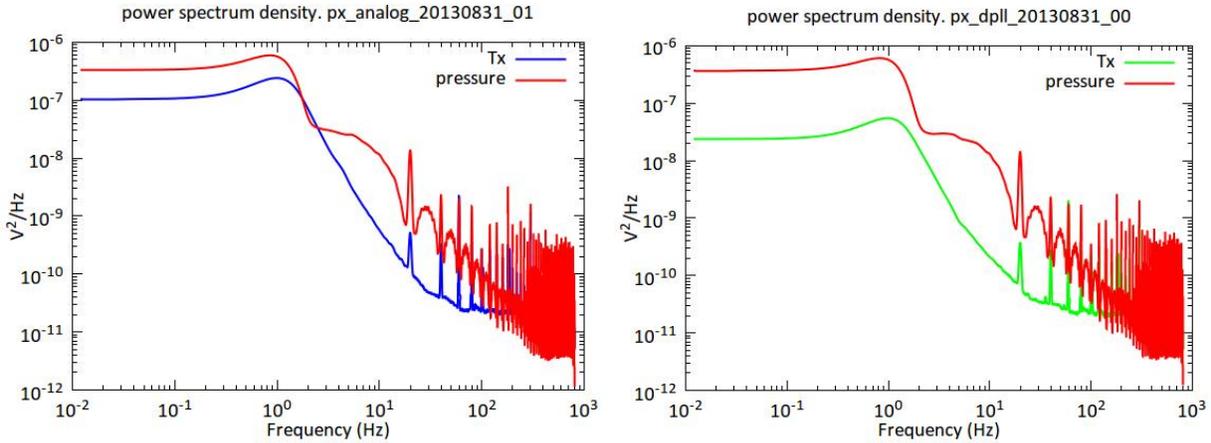


Figure 6. Spectral density (PSD) for digital PLL (a), and original analog PLL (b)

(Using Welch algorithm with 128*1024 long window).

Red is pressure, blue is transmitted power (Volts from the detector diode).

Next step was to analyze the frequency distribution of noise in the transmitted power and pressure. We sampled these signals at a rate of 50 kHz, and then applied Welch algorithm to plot the power spectral density (PSD). (fig.6) As we can observe, noise is correlated for this case. Remarkably, pressure and transmitted power spectra repeat each other's trend, however with a slightly less amplitude of harmonics for the case of transmitted power.

If we compare both of the circuits explicitly (Figure 7), we see that both of the components result in the similar frequency distribution of the noise, present in transmitted power. However, the amplitude in the case of digital control is less, especially at a low-frequency region. Both of the boards have a cut-off frequency of about 10 Hz.

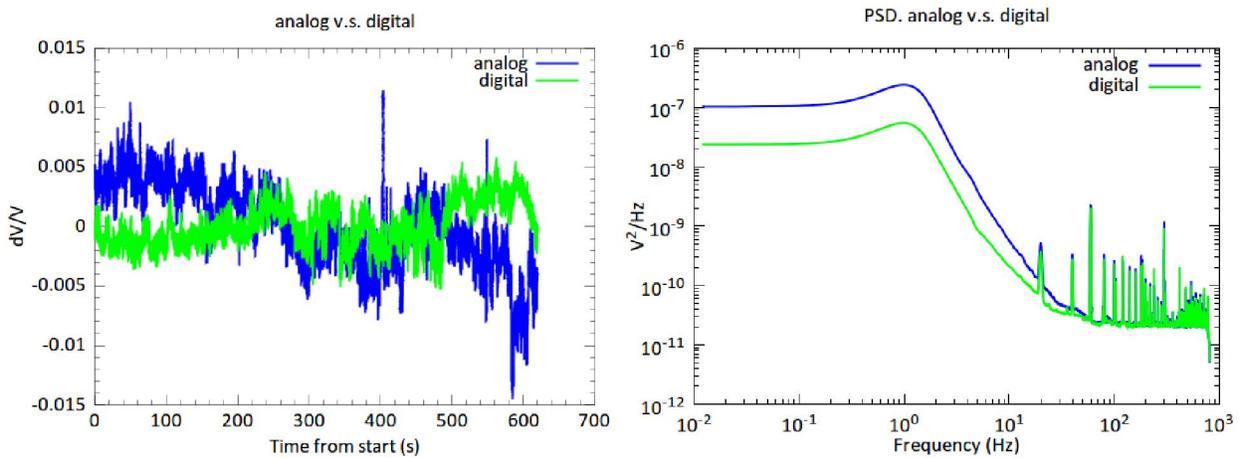


Figure 7. Comparison of transmitted power noise in the cavity with digital PLL and original analog PLL

Relative deviation (a) and PSD (b); (start times for analog and digital measurements were different)

Conclusion

Thus, a digital phase control based on FPGA board for VTS LLRF was developed. It was initially developed for microphonics studies, however it also performed well on the VTS.

The following board demonstrated the performance comparable with that of the original analog PLL. However the designed board showed a better, closer to ideal, uniform spectrum distribution.

The designed PLL has much easier gain control over the original one. It also supports control from LabView, so it may be easily plugged into the current VTS control system.

There was also 1 kHz modulation of the digital PLL output present. This was not caused by the digital board itself, and there was no such a modulation in the original board. Thus maybe it is a better sensitivity of the digital board that responses to some of the rapidly changing external phenomena (microphonics, etc). It is usually the case that digital PLLs are better than analog ones in terms of less tracking jitter and phase noise.

Acknowledgments:

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I would like to thank my colleague Dmitry Sergatskov for helping us to conduct tests and analyze data on VTS.

I would also like to thank the whole SRF department for giving us a chance to test our component on VTS.

Supplementary materials

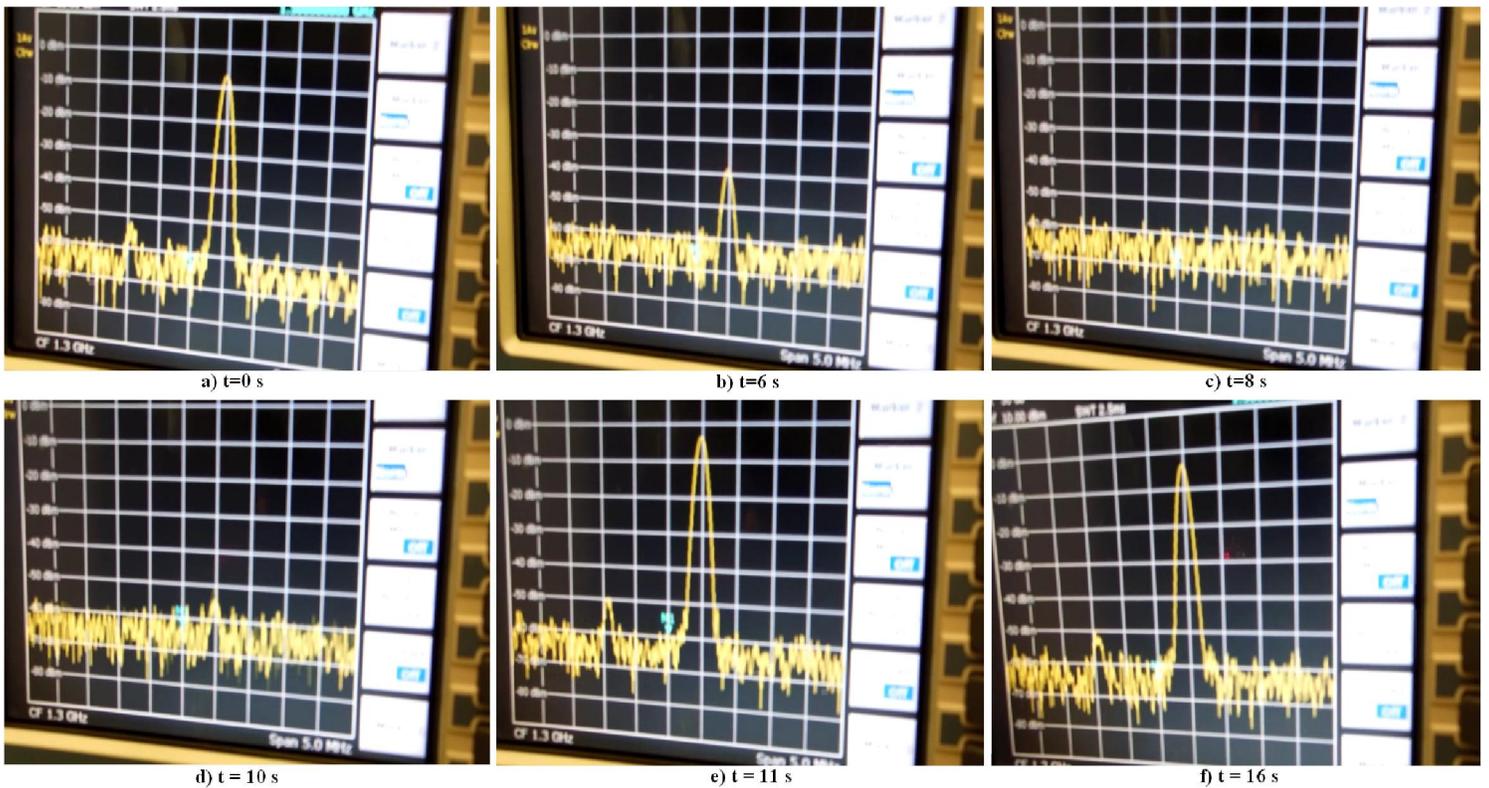


Figure 8. Evolution of the probe signal on VTS LLRF scope:

- The analog PLL is about to be unplugged from the FM Agilent source
- 6 s after unplugging of analog PLL; the cavity gradually goes off resonance
- 8 s after unplugging analog PLL: no resonance signal detected on the scope
- The digital board is about to be plugged into the Agilent FM
- Digital PLL is plugged; cavity is on resonance
- The system is stable