

FPGA BEAM LOSS MONITOR SYSTEM FOR THE SRF FACILITY

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ABSTRACT

A Field Programmable Gate Array (FPGA)-based Time-to-Digital Converter (TDC) is being developed for use with cryogenic ionization chamber beam loss monitors which have been proposed for installation inside the cryostats at the Superconducting Radio-Frequency (SRF) beam test facility at Fermilab. The scheme employs an Altera Cyclone III FPGA and He-ionization chambers with recycling integrators as dose rate monitors. The time intervals between the pulses out from the dose rate monitors are measured with high timing resolution (> 10 bits) using this TDC method. This provides a more accurate measure of the current than was previously possible. The FPGA was initially programmed with a single channel output for test purposes; however several additional channels are required for the final phase. This project has extended the new design to handle multiple channel output up to 8 channels with a timing resolution of 1ns (nanosecond). This project discusses the design and test results that we have obtained so far.

Key words: Beam loss monitors, FPGA, SRF, Time-to-Digital Converter

Introduction

Fermilab's mission of understanding the nature of matter and energy is conducted by high energy particle physics research. A particle accelerator is one of the tools to understand the nature of matter and energy by making multiple collisions at different points of the ring or linear machine while recollecting enough data for studies and recognition of new particles. The Superconducting Radio-Frequency (SRF) beam test facility at Fermilab proposes projects that provide a new vision and mission for the lab. Fermilab has the world's second largest particle collider: the Tevatron, a 6.28 km storage ring that accelerates particles up to 1 TeV. All this massive and high production of energy will not be possible without many components and systems that are in the accelerator.

One of the most important systems needed while the Tevatron and many other accelerators are producing beam is the beam loss monitor (BLM) system. The beam produced by an accelerator machine needs to be focused in a determined shape, therefore the use of magnets such as quadrupole, dipole and correction magnets is needed taking into account that for a better functionality in some accelerators they must be cooled to cryogenic temperatures. This beam is really powerful and generates losses that can induce damage to the magnets and components in the machine due to the stray radiation. BLM systems at Fermilab have been developed since approximately 1981 mainly to protect the magnets, components and to prevent unexpected shut-downs. The BLM system for the SRF beam test facility department includes a Field Programmable Gate Array (FPGA)-based Time-to-Digital Converter (TDC) and a He-Ionization Chamber. In the construction of BLM systems, it is extremely important to highlight the features and the operation conditions of the accelerator. The SRF beam test facility needs a digital BLM that can react to losses at different time scales. This project extends the functionality of the FPGA-TDC from one channel output into an eight channels with a timing resolution of 1ns for the final cryogenic BLM system.

Beam loss Monitors

A beam produced by an accelerator machine generates high levels of radiation, hence different types of losses are constantly in the storage ring or linear machines which can affect the components, the magnets special functionality and can also provoke unexpected shut-downs. The BLM systems make emphasis on the recognition of quantity and location of the loss. There exist two types of losses, fast and slow. A fast loss is the one that is presented during a few turns of the beam. Generally the BLM is not used to detect those losses due to other detectable errors that can appear such as closed vacuums or broken supplies, but the BLM system warns of an intolerable loss. A slow loss is determined over time in the storage rings or over distance on the linear machines. The BLM reacts to these kinds of losses which helps to understand the machine's behavior and prevents quenches caused by an overtime loss. As in many systems, there are different types and techniques used for a BLM. The most common ones are: Ionization Chamber, Scintillation Counter, Electron Multipliers, Cryogenic Calorimeter and PIN Photodiodes.

The SRF beam test facility department is working on multiple projects. One such project is to develop an advanced system that includes new vacuums, RF cavities, Toroids and BLM systems for better operations in the accelerators. The development on SRF projects takes place mainly in the A0 Lab and New Muon Lab (NML) while this project improves the functionality of the Altera Cyclone III FPGA in the BLM system by extending the design of the output signals.

Materials and Methods

He-Ionization Chamber

This is a metal construction chamber, a ceramic insulator which contains the signal electrode. This device is filled with Helium, and its current is proportional to the dose rate monitor (recycling integrator (RI)). This cryogenic beam loss monitor operates from 5K to 350K in air and high vacuum, is a radiation-hard design, and it does not require maintenance. Figure 1 displays the He-Ionization Chamber with its recycling integrator.

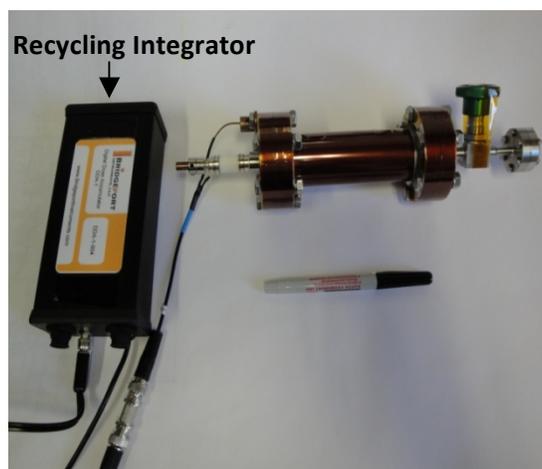


Figure 1 He-Ionization Chamber and recycling integrator

FPGA Altera Cyclone III Starter Board EP3C25F324-C8

First of all, an FPGA is a semiconductor device that can be programmed after its fabrication, which means that this device allows the programmer to access the product features, adapt it to new standards and reconfigure the hardware for specific applications (field-programmable). FPGAs nowadays have mixes of embedded SRAM, high-speed I/Os, logic blocks, high-speed transceivers, and routing. For the SRF proposed project the Cyclone III Starter Board FPGA is the chosen one due to the combination of low cost, high functionality, and power optimization that maximize the competitive edge. The schematic view of this board is shown below on figure 2.

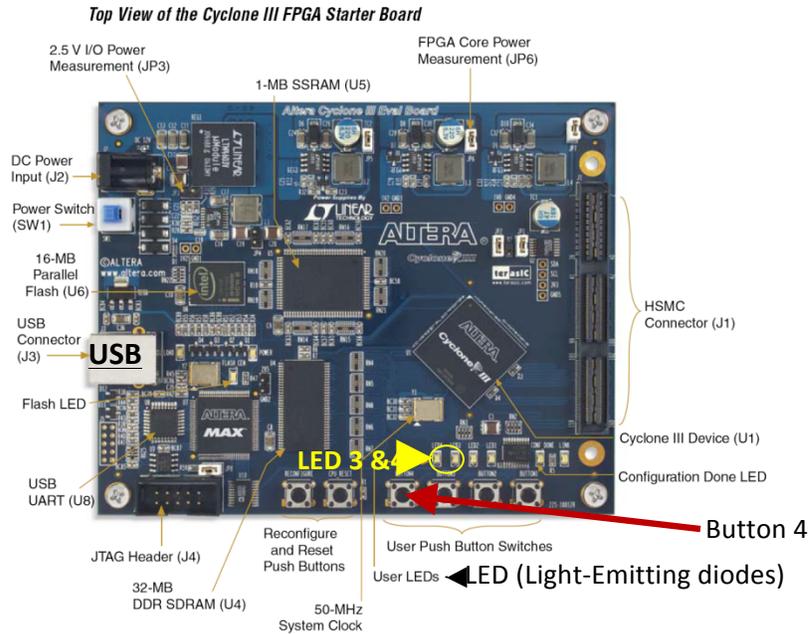


Figure 2 Altera Cyclone III FPGA

Cryogenic BLM description and testing

Multiple bench-top measurements from the recycling integrator are needed to make sure that the current-to-frequency conversion is generated in the dynamic range needed. The TDC method and the dynamic range assure high timing resolution (> 10 bits).

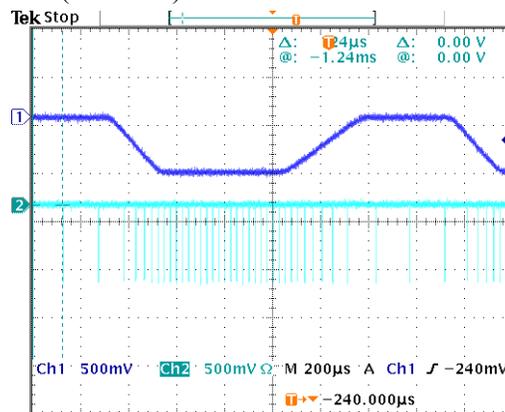


Figure 3 Scope picture from the recycling integrator testing

In Figure 3, Ch 1 represents the current input and Ch2 the output pulses from the DDA, where it is possible to observe that the recycling integrator will show multiple pulses from the input current helping the BLM system to have a better response.

After the RI dynamic range is measured, the He-ion chamber is installed in the A0 beam line (A0 Lab). The signal output from the recycling integrator is connected to the control room. This connection branches between the main computer and a scope. The scope signal is connected to a Fan-in/Fan-out unit which will take this signal to a NIM-to-LVDS module. After the signal is converted the module deliver the new signal to the FPGA where the Synchronous Static Random Access Memory (SSRAM) will read and write (storage) the information of the loss only after the button 4 is pressed. The FPGA has to be connected to a computer (preferable a laptop) while the memory is recording the data. This process uses Terasic Control Panel which takes the information into a text file. This data is recorded in hexadecimal and the use of an excel file is needed to analyze and graph the losses detected from the He-ionization chamber.

The Cyclone III Altera FPGA uses Quartus II Web Edition as the design software. The single channel output design is based on schematics language, where the time resolution of 1 nanosecond takes place in the TDC block which converts the signal into digital representation using four clock phases where the exact location of the leading and falling edge will be recorded. It is important to highlight that in this design the use of VHDL or Verilog was not necessary due to the actions needed from the FPGA. For other purposes with FPGAs the best hardware description languages are the ones previously mentioned. Regardless of the language used for a new design on this kind of device, it is highly recommended to connect at least one LED (Light-emitting diode) which will show the low-level operational in FPGA. It is easy to determine how useful a firmware is on the FPGAs, simply by noticing if the LED is blinking or not. The blinking indicates that most of the important details have been designed correctly, such as the ground pins, mode setting and compiler software setting, etc. “The LED blinking firmware in the FPGA design is as essential as the ‘hello world’ program in the C programming language”¹.

Extension of the design

For the final phase of the cryogenic BLM system on the SRF project, the signal output requires multiple channels. Hence, it was determined to have an initial extension of eight channels.

This new design development has a base design (single channel) which is already established and has worked with the BLM system. Nevertheless, the process has to be very careful making sure that the time-to-digital converter will still work in the new design as the primary tool from the FPGA. The eight channel schematics design main block window will not have many differences from the single channel, because the main functionality needed from the firmware is the same. Generating multiple channels require the creation of a block which will include the functionality of the single channel branching into eight outputs with parameterized multiplexers (Altera functions). To create a new block it is always recommended to use a block previously used, then do the necessary changes such as name, configuration, inputs, outputs, etc. The display of “MultiCh1” the new block created for this extension goes as follows: inputs, eight single channels blocks, two multiplexers, two storage blocks and outputs. Why two multiplexer and two storage blocks? Because the FPGA firmware now needs to storage the leading and

¹ Hartmut F.-W. Sadrozinski, and Jin-Yuan Wu, *Application of Field-Programmable Gate Arrays in Scientific Research*. Taylor and Francis Group, LLC, 2011, *chapter four “Examples of an FPGA in daily design jobs”*.

the falling edge from each pulse before it can be written down into the SSRAM. On the previous design, this procedure was not necessary due to the straight forward functionality. The multiple channels design in the FPGA has to be more assertive with the data selection for each channel. The main block window difference between the single and the multiple channels designs is shown in Figure 4 and 5.

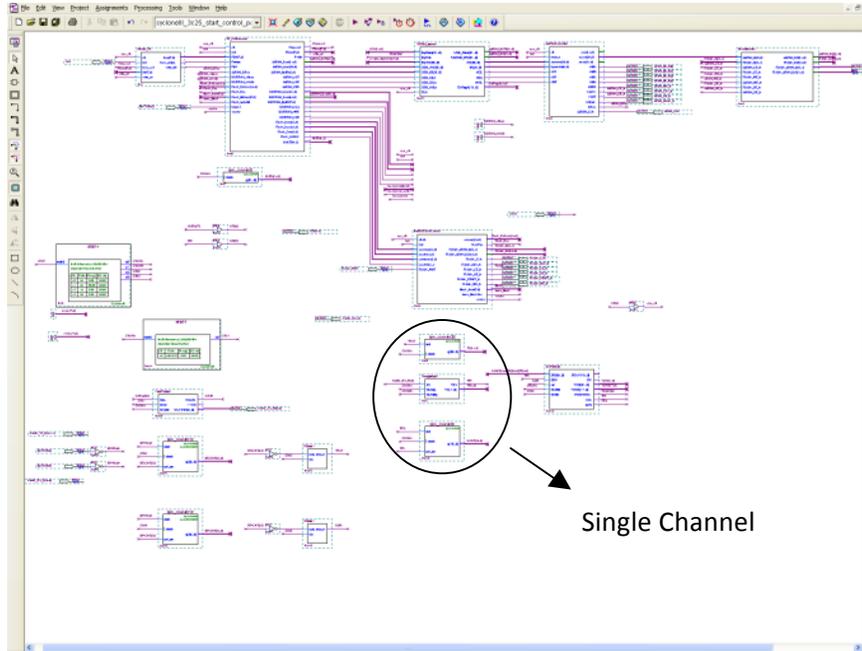


Figure 4 Main Block Window Single Channel Design

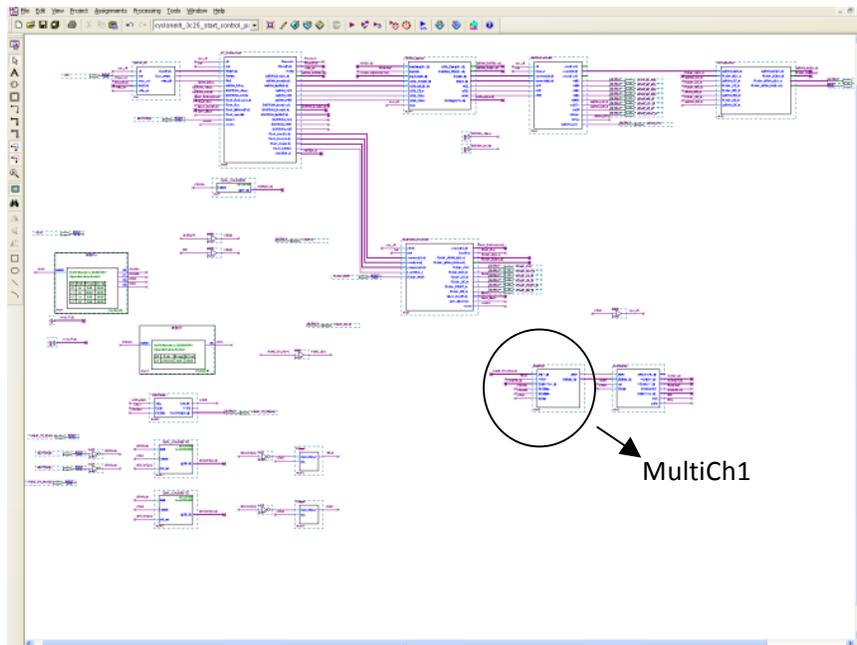


Figure 5 Main Block Window Eight Channel Design

Multiple Channel Design Testing

After a design is finished and compiled by Quartus, the most important step is to reconfigure the flash memory. This will reset the firmware of the FPGA and it will allow the tester to prove the functionality of the new design. The first thing to look about the firmware, as is mentioned before in this paper, is to make sure that at least one LED is blinking to determine that the design is correct. After this simple inspection, it is necessary the use of pulse generators to locate mistakes in the read-out of the data. The process of extracting information initiates by accessing the SSRAM memory. Then counters and clocks are needed to determine when it is time to read and write the information. In the new and single channel design it has been assigned that the LED 3 will be blinking all the time and that the LED 4 will go off. A 'switch' button 4, is pressed to give the sign to the SSRAM to start recording data. When this LED 4 goes on, means that the recollection of data is done. The time given for the memory to record data is approximately 80 seconds with full memory length. This is controlled by a counter located in the main block window of the designs. Taking into account that for some test, the memory length is modified, the time will vary. The use of pulse generators helps to assure if the firmware is working properly. This data comes from a text file produce by Terasic, which will be uploaded into the excel file that help analyzing data with formulas and graphs. The most important procedure for the new design is the computation of the standard deviation (σ) which helps to determine whether each channel is recording data properly or not. This file uses formulas that convert the hexadecimal number, determine the current, calculate the width and measure the distance between pulses. The standard deviation shows if the time difference between pulses is very close or big differences are measured. A small standard deviation (from 0 to 0.28) means that the desired data was achieved, and if it exceeds 0.28, this means that the channel needs to be recompiled.

Results

Single Channel

The following are the results obtained from the single channel firmware when a magnet was swiped twice in the A0 beam line.

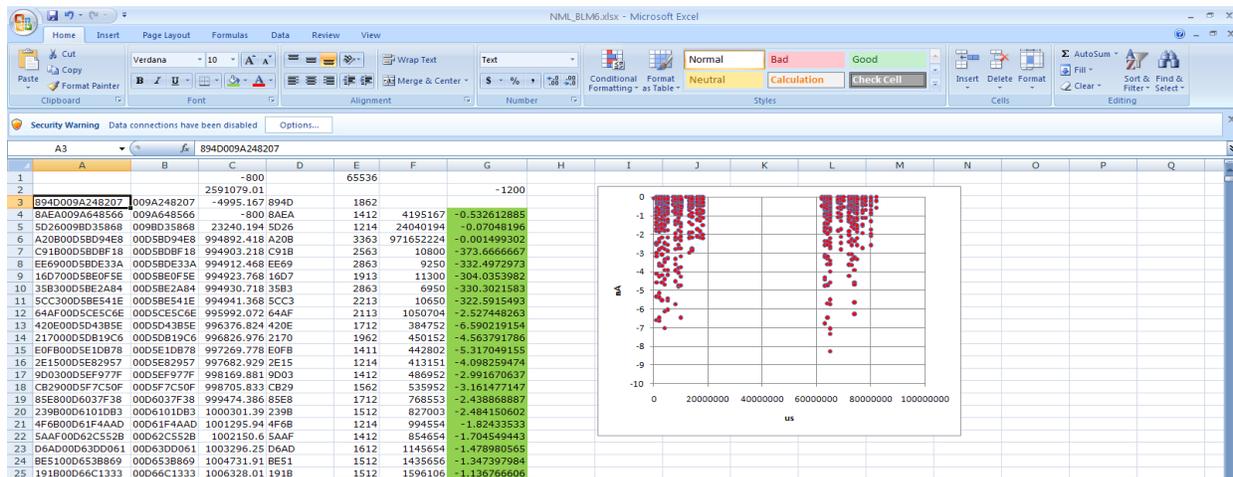


Figure 6 Excel File view with the single design analysis

In Figure 6, the functionality of excel can be proven. The ‘G’ or seventh row gives the current of each pulse. The other rows are used to convert the hexadecimal number and calculate the width and the time difference between pulses.

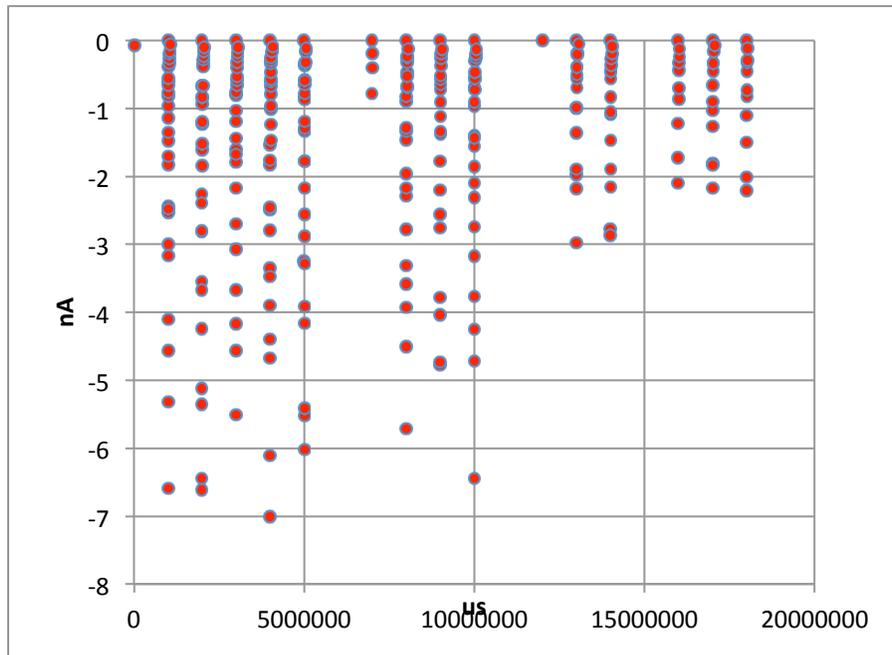


Figure 7 First Swipe of the magnet

Figure 7 is a closest view of the first swipe of the magnet. The beam loss was seen at 1 Hz frequency, and thanks to the TDC, every pulse (dots) can be seen on the graph.

Multiple Channels

Three different pulse generators were use in the testing of the eight (extension) design and these are the results:

	Ch 1	Ch 2	Ch 3	Ch 4	Ch 5	Ch 6	Ch 7	Ch 8
Digital pulse generator	0.25711	0.25732	26126.65816	32651756242	0.257108964	0.25731747	0.25731747	15660542420
Hewlett Packard (HP) pulse generator	413.66	33845.2	60426240484	9684311346	57125399184	35083168195	67936483122	65286098509
Berkeley Nucleonics Corporation (BNC) pulse generator	3344.38	33845.2	0.230145	54863652917	71344979451	59789000409	0.241546	61943725340

Table 1 Standard deviation table

Table 1 highlighted cells represents the non acceptable standard deviations calculated for each channel using excel’s formulas. The test with the regular pulse generators presented more defective channels than the digital one; hence the finals tests will be with the last pulse generator mentioned.

Conclusion

This project has discussed the methods used to test the FPGA-based TDC for a BLM system. The objective needed from SRF was to have multiple outputs from the He-ionization chamber DDA. From the results, we can conclude that the objective is partially achieved due to missing of acceptable standard deviations from some channels. So far, the new design achieved the most important feature, the time resolution of 1ns is working. Future work in this design is to find the exact problem in channels 3, 4 and 8. Then the final test for this extension will be reading output from the He-Ionization chamber.

Finally, we can conclude by saying that extension of designs on FPGAs is possible, especially the ones manufactured by Altera. Regardless of the missing steps for the final testing on the new FPGA firmware, we can affirm that progress has been made for the SRF cryogenic beam loss monitor system this summer.

Acknowledgements

First I would like to show my deep gratitude to Dianne Engram, Jamieson Olsen, Linda Diepholz and the entire SIST committee for allowing me to acquire such valuable experience. Also, a special thanks to my supervisor Jin-Yuan Wu, and Arden Warner who guide me throughout the project development stages. I would also thank Fermilab employees, and highlight the fourteenth floor Particle Physics Division staff for the enjoyable and full of knowledge environment given during these amazing twelve weeks.

Finally, I would like to thank my mentors David Peterson and Elmie Peoples, and to Dr. Davenport for all the support given in the paper and presentation development. Thanks Fermilab for this unforgettable summer.

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