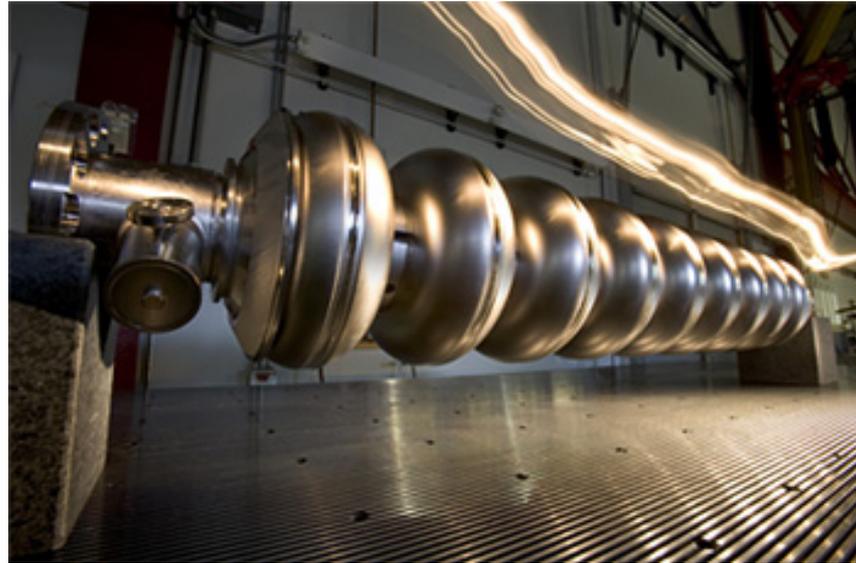


Control of detuning in superconducting cavities



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Final summer student meeting
08/27/2013

Outline

- Introduction to detuning of the cavities
- How to control detuning
- Components for signal processing.
- LLRF Test at Vertical Test Stand (VTS)
- Real Cavity Simulator

Detuning in cavities

Sources:

1. Lorentz force detuning

- deterministic nature:
- contracting the cell near iris

$$\frac{\omega_0 - \omega}{\omega_0} = \frac{\int_V (\epsilon_0 |\vec{E}_0|^2 - \mu_0 |\vec{H}_0|^2) dV}{\int_V (\epsilon_0 |\vec{E}_0|^2 + \mu_0 |\vec{H}_0|^2) dV}$$

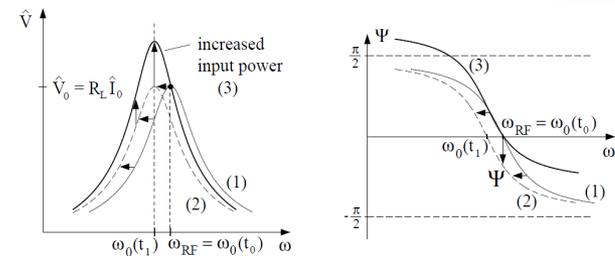
2. Microphonics

- stochastic process
- sources: helium pressure variations (~1 Hz), machinery, traffic
- mechanical bandwidth of noise up to 1 kHz

Compensation methods:

1. Adjusting the input power:

- stochastic process
- Energy consuming
- Costs for SC accelerator are increased by 10% to 20%



2. Feedback or feed-forward with piezo:

- Latency up to 1 ms
- Resolution 1/100 nm



Nallatech Virtex-4 board

Xilinx Virtex-4 SX35:

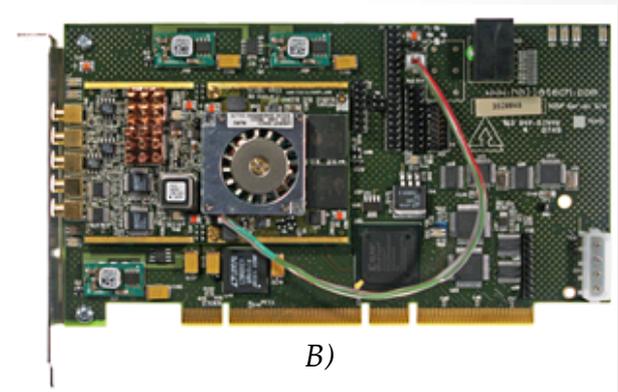
- 2 independent 14 bits/105 MSPS ADC channels
- 2 independent 14 bits/160 MSPS DAC channels
- Built-in 18 bit multiplier and 48 bit accumulator
- FPGA re-programmable chip
- Internal(100 MHz) and external clock
- Low-level VHDL programming language
- C callable libraries
- Custom Matlab wrapper

Major signal processing VHDL components:

- Numerically Controlled Oscillator
- Mixer
- Filter



A)

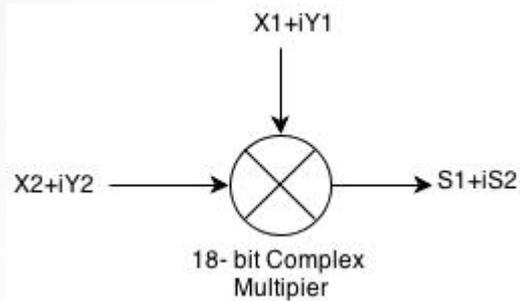


B)

Xilinx® XtremeDSP Development Kit, Virtex-4 Edition.

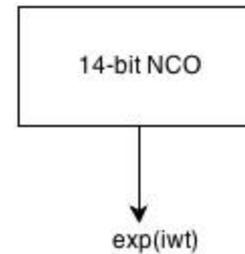
A) With case. B) Without case

Mixer



- 18 bit precision complex multiplication
- $M = (X_1-iY_1) \times (X_2+iY_2)$
- Works at a clock cycle

Numerically Controlled Oscillator (NCO)



- 14-bit precision cosine, sine output
- Based on counter-driven lookup table
- 240 mHz resolution
- Adjustable frequency
- AM, FM inputs (optional)

Filter/Cavity simulator

$$X_k = X_{k+1}(1 - dt/\tau) + U \sim X_{k+1} \exp(-dt/\tau) + U;$$
$$X_0 = 0;$$

$$dt/\tau \ll 1$$

dt – clock period

tau – time constant of the filter

U – 14 bit input

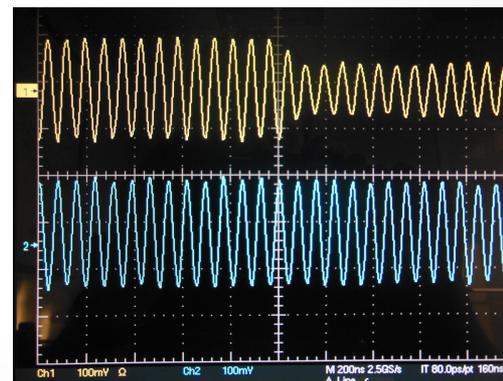
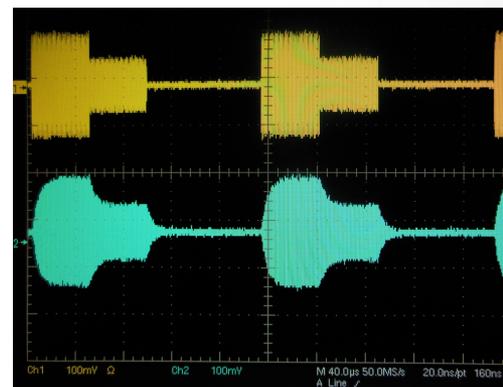
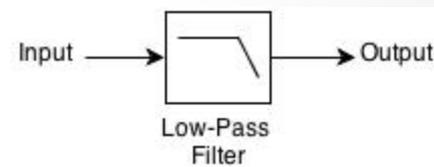
X – 32 bit accumulator

Inputs:

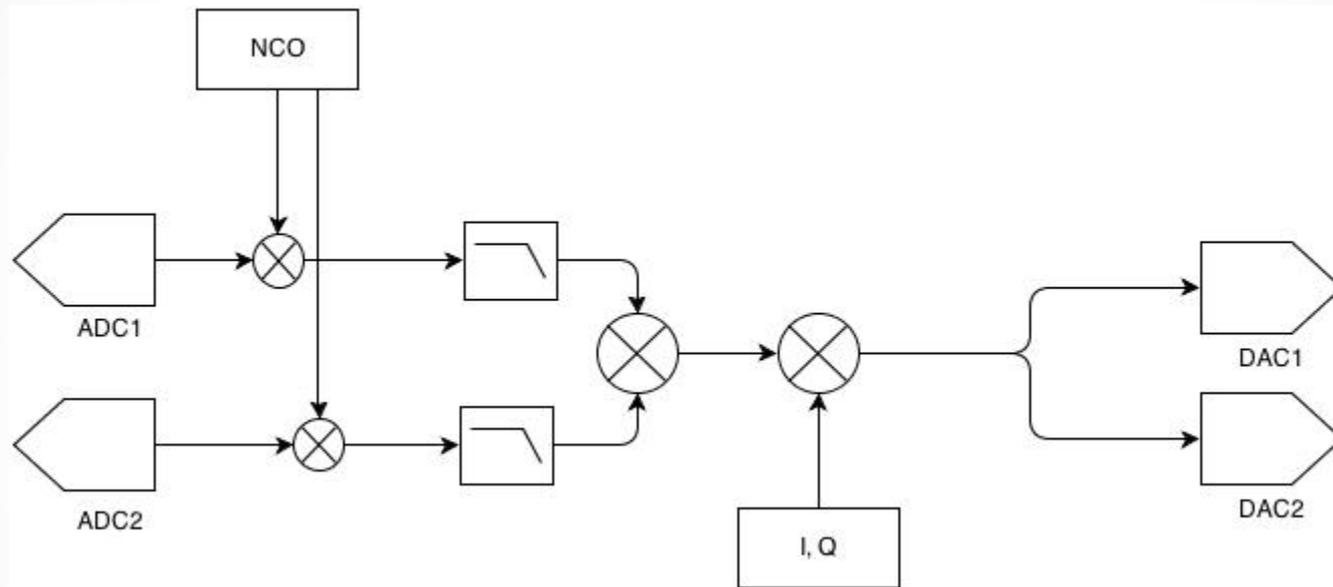
- Incoming signal
- Cut-off frequency (range 10Hz – 10KHz)
- Gain

Outputs:

- Filtered signal (up to 30 bit precision)

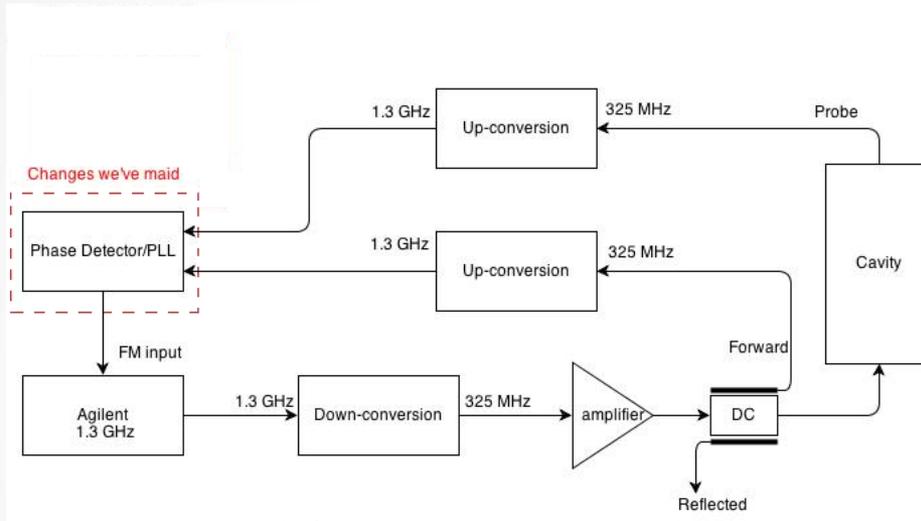


Phase difference meter



- Developed for microphonics control
- Exactly the same components were used to build a real-time simulator

Vertical Test Stand Low-Level-RF



Simplified VTS LLRF scheme



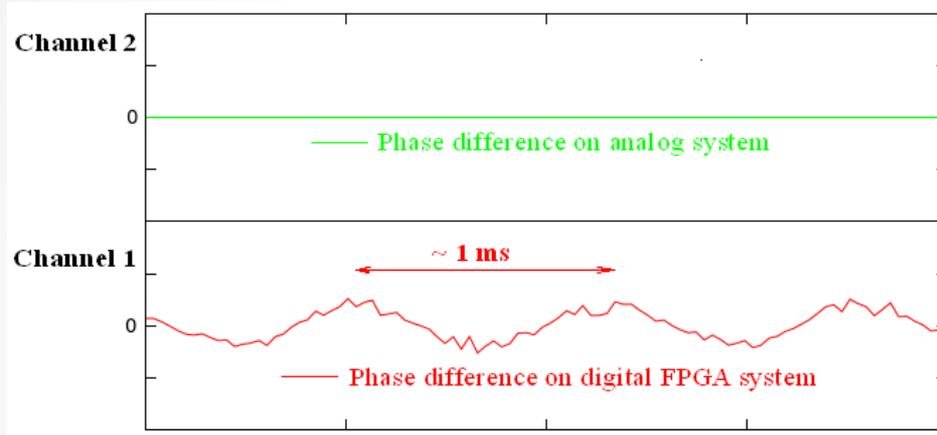
VTS LLRF control facility

Changes we have made:

Analog PLL (1.3 Ghz) ->

AD/LLRF Transceiver (1.3 Ghz -> 13 Mhz) + FPGA PLL(13 Mhz)

Phase and gain adjustment



Indications on the scope



Coaxial trombone

- Trombone was used for phase shifting
- Gain was adjusted so that phase signals for digital and analog system behaved similarly.
- Digital system had 1 kHz oscillations, that did not depend on cut-off frequency of FPGA filters.

Results of LLRF test

id	52296
timestamp	2013-08-23 19:50:58.0
alert	no
type	manual
author	Dmitri Sergatskov
device	VTS-1/SIH-NR-111
stand	VTS
log	MTF
categories	Superconducting Device
systems	Power/Quench Studies
keywords	Status Report
title	warm up vts1

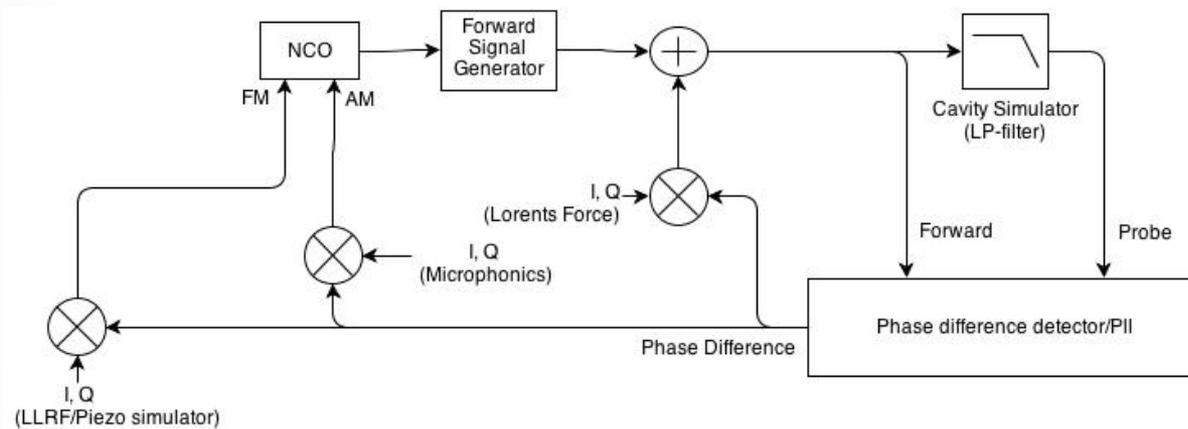
We done with cavity tests and digital PLL (DPLL) tests.
DPLL appears to be working much better than what we have at the moment at VTS!

Please warm up the cryostat by Monday.

- Comparable performance of digital PLL and analog PLL
- Much easier control of digital PLL
- 1kHz modulation present at digital PLL need to be investigated (microphonics?)
- SRF meeting talk on August, 26th

What can we do next?

- Careful performance measurements of all the components with using Simulator:



- Substitute 1.3 GHz NCO/transceiver for Agilent by FPGA 13 MHz NCO + AD/LLRF Transceiver
- Introduce AM-modulation for precise Q_0 -measurements

Conclusion

- The signal processing VHDL components were designed (Mixer, Filter, Precise NCO, PLL, Cavity Simulator)
- Successful digital PLL tests on VTS LLRF.