

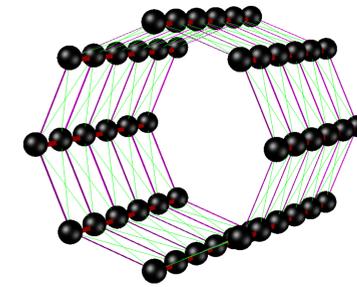
Performance Study of High Speed Data Communication for CMS Tracking Trigger Demonstration

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Introduction

The High Luminosity LHC (HL-LHC) poses real challenges for silicon based track trigger systems, due to huge data volume with more than 100 Tbps bandwidth required, and extremely short processing latency available (few microseconds). Because of that, Fermilab has launched an aggressive R&D program to develop such a tracking trigger system. Part of this program is the development and construction of a Vertical Slice Demonstration System. It will comprise a full tracking trigger path, running at full speed with simulated high-luminosity data to measure trigger latency and efficiency, to study overall system performance and to identify appropriate solutions to possible bottlenecks. The success of this project will provide the needed proof-of-existence of a L1 silicon-based tracking trigger for HL-LHC, and will allow the design of the upgraded tracker to be finalized. The project will directly and visibly impact the quality of physics results produced at the HL-LHC.

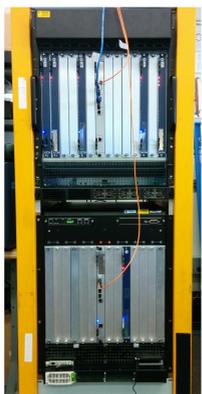
The main purpose of this study is to evaluate the performance of high speed data communication channels of the Pulsar IIb board, which is the workhorse of the demonstration system. The result of such evaluation will be used for the Data Sourcing sub-system in the demonstration.



Conceptual view of the proposed CMS phase II L1 tracking trigger towers. Each node in this diagram represents a trigger tower processor engine. Within each processor engine crate the full mesh backplane is used for time multiplexing of the incoming data, while the simple data sharing is handled with inter-crate links.

Hardware Overview

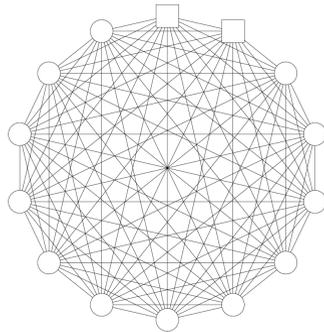
- The Advanced Telecommunications Computing Architecture (ATCA) platform with a Full Mesh 14-slot backplane is chosen for our studies.
- Switch boards can reside in slots 1 and 2 and implement a 10G or 40Gb/s Ethernet network.



This photo left shows a rack with two crates (up and down). Each has 14 slots.

Full Mesh backplanes enable communication between every slot, with no switching or blocking.

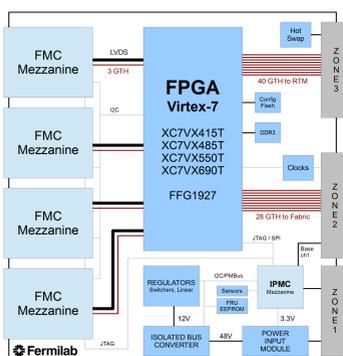
Each line in the diagram to the right represents a channel which consists of up to four bidirectional ports (lanes).



The Pulsar IIb Board

To address the silicon based track trigger needs described above, our design goal is to create a uniquely scalable architecture abundant in flexible, non-blocking, high bandwidth board to board communication channels while keeping the design as simple as possible.

The Pulsar IIb is designed around one big Virtex-7 Field Programmable Gate Array (FPGA).



This board features:

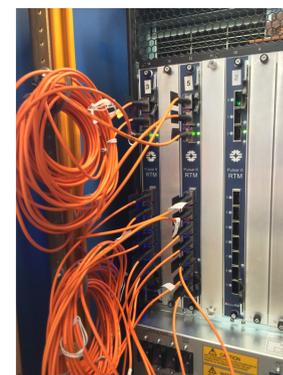
- 80 GTH serial transceivers with each at up to 10 Gbps for fabric, Rear Transition Module (RTM) and Mezzanine cards.
- Four FMC Mezzanine card slots.



Scheme of the Pulsar IIb board (left). Above is a picture of the board and the RTM.

Pulsar IIb link performance

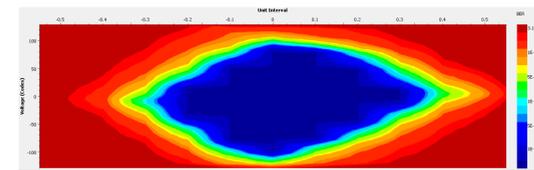
The board is programmed with IBERT link test firmware at 6.25, 8 and 10 Gbps speed rates. On the RTM, pairs of Quad Small Form-factor Pluggable (QSFP+) transceivers are connected, linking pairs of modules in one or two boards. The quality of the links is evaluated using statistical eye diagrams that measure the tolerance of



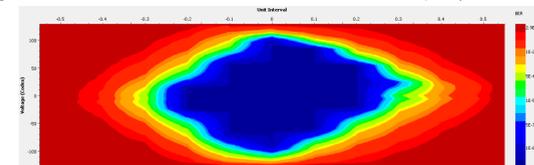
Possible link setup on the RTMs, connecting two boards.

the system to offset samples of the data sent. The color on the diagram represents a logarithmic scale on Bit Error Ratio (BER) values. In general, as we increase the speed of the data link, several factors influence link performance such as: cross talk, impedance mismatch, reflections and attenuation. The performance can be optimized by parameter tuning to increase the Open Area in the eye diagrams. For example, one can tune parameters such as the amplitude of the LVDS signal of the transmitter (TX Diff Swing), the pre-cursor and post-cursor emphases. Examples of eye diagrams are shown on the left.

In addition, different type of fiber cables (3M and Molex) have been used for testing, and the 3M cables performed better and will be used for the demonstration. The conclusion of the study is that the Pulsar IIb data communication performance is good enough to meet the demonstration requirements.

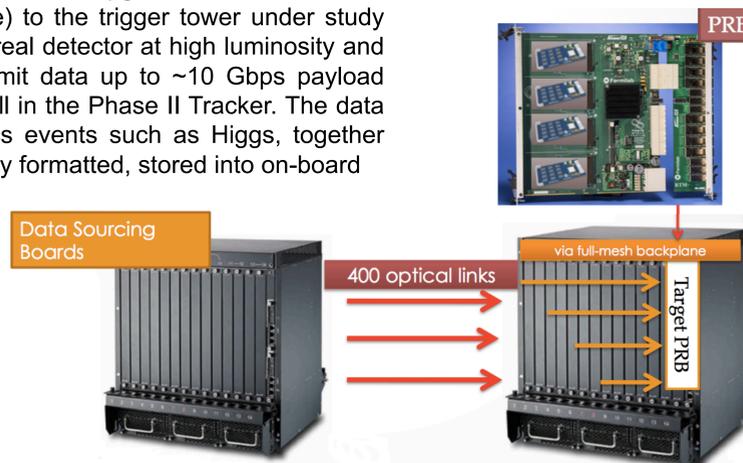


Eye diagrams for two different channels at 10 Gbps (one direction).

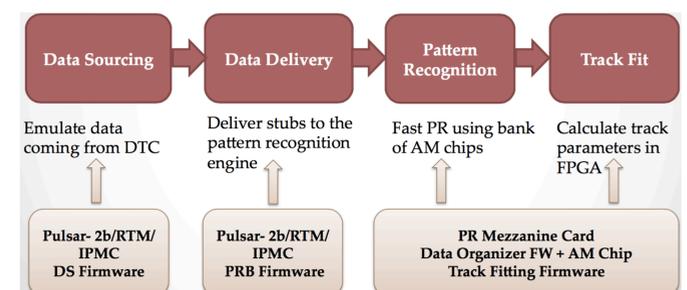


Data Sourcing

The Data Source mimics the data flow out of the upgraded Phase II outer-tracker. It will drive ~400 fibers (one/module) to the trigger tower under study exactly as if the data were coming from the real detector at high luminosity and full speed. Each fiber connection will transmit data up to ~10 Gbps payload bandwidth, in the same way that modules will in the Phase II Tracker. The data will be derived from simulation (with physics events such as Higgs, together with hundreds of pileup events), appropriately formatted, stored into on-board memories, and then played back at full speed. The Pulsar IIb can be used for the Data Source stage, as each board has 40 optical interfaces on the RTM (all bi-directional, but only one direction is needed). Ten Pulsar IIb boards can source ~400 modules worth of data (one trigger tower). Demonstrations of the triggering system are being prepared following this scheme.



Stages of the demonstration system using Data Sourcing.



In order to prepare the hardware for Data Sourcing demonstrations, IBERT link test firmware has been used to evaluate the communication performance between two boards, with the information flowing in one direction. The links are stable at 10Gbps, and have been tested at Bit Error Ratios down to 10^{-14} .