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Performance Study of High Speed Data Communication for CMS Tracking Trigger Demonstration

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Internship final presentation

05 August 2015

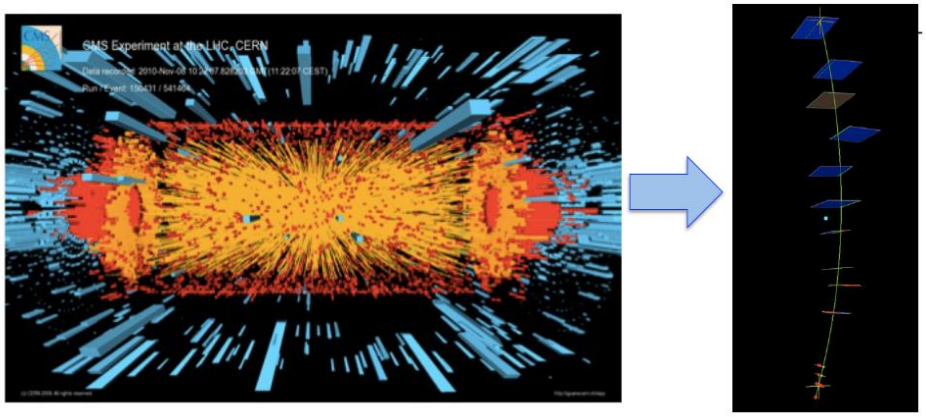
Outline

- **Introduction.**
- Hardware description.
- Overview of the demonstration system.
- Pulsar IIb board link performance.
- Summary.

New Tracking Trigger System for CMS @ HL-LHC

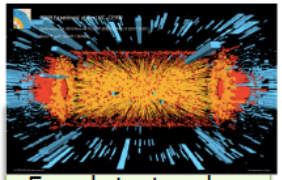
High Luminosity: ten-fold increase in collision rate.

- Huge data volume ⟶ High speed (more than 100 Tbps bw required).
- Short processing latency (few microseconds).

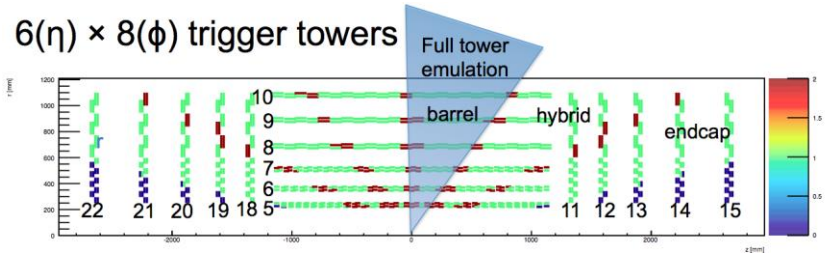


Fermilab launched a R&D program to develop the new tracking trigger system for CMS. Part of this program is the development and construction of a Demonstration System.

Stages of the Demonstration System



Emulate tracker output using HL-LHC simulation data



Partition detector into trigger towers

High speed data transfer!

Associative Memory (AM) PR approach

Processing Latency Δ t

Goal: ~4 µs

Data formatting / delivery

Δt1

Pattern Recognition (PR)

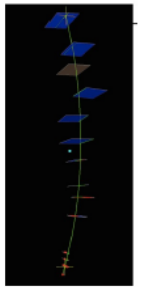
Finer pattern recognition

Δt2

Track Fitting

Δt3

Tracks out



2015: Initial board level latency measurements/study.
2016: Move towards system/tower level demonstrations.

- Demonstrate feasibility of TT.
- Identify real bottlenecks and guide R&D.

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Towards a Tracking Trigger Demonstration

Stages:

- **2013: Demonstration concept development.**
- **2014: Paving the way for demonstration.**
- **2015: Beginning of demonstration at board level.**
- 2016: System level/trigger tower demonstration.
- 2017: More performance studies/extrapolations, TDR.

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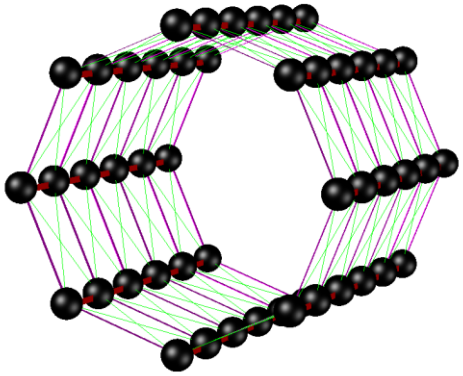
Hardware for the Tracking Trigger system

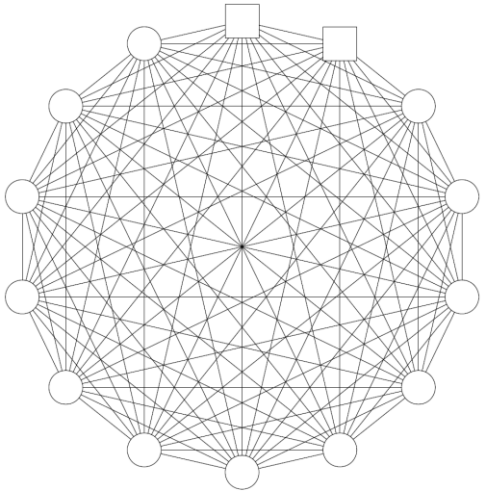


Conceptual view of the proposed CMS phase II L1 tracking trigger towers.

- Each node represents a trigger tower processor engine.
- Within each processor engine crate the full mesh backplane is used for time multiplexing of the incoming data.

Diagram of the internal connections in a processing node.

- Full Mesh backplanes enable communication between every slot, with no switching or blocking.
- Each line in the diagram represents a channel which consists of up to four bidirectional ports (lanes).



Hardware for the Tracking Trigger system

ATCA rack with two crates (up and down). Each crate has 14 slots: 2 for switches and 12 for Pattern Recognition Boards (PRBs), which are in charge of the data processing. Only 10 PRBs used in the demonstration.

Down, a picture of the Pulsar IIb and the Rear Transition Module (RTM), the latter communicates data to the optic fiber transceivers.
Near 1 Tbps total (all transceivers within the board).

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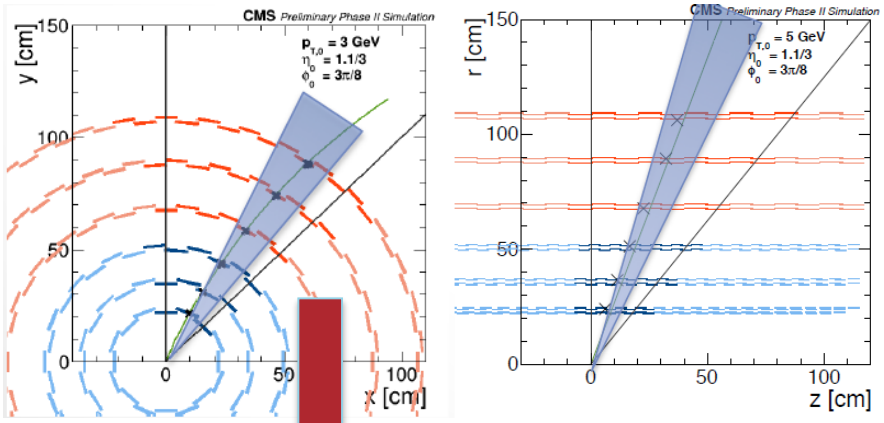
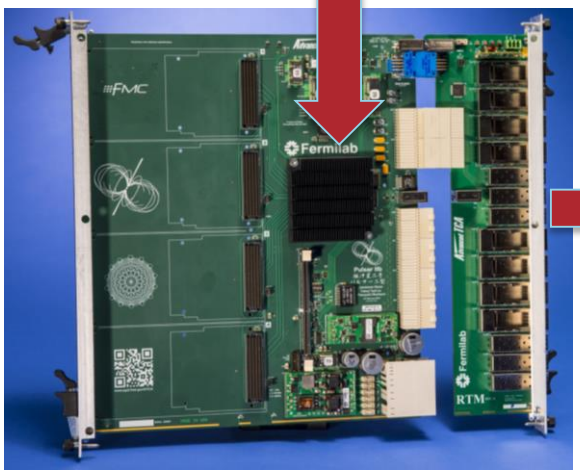
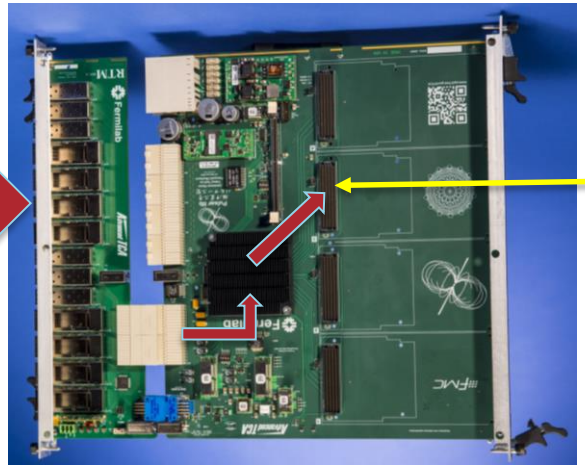
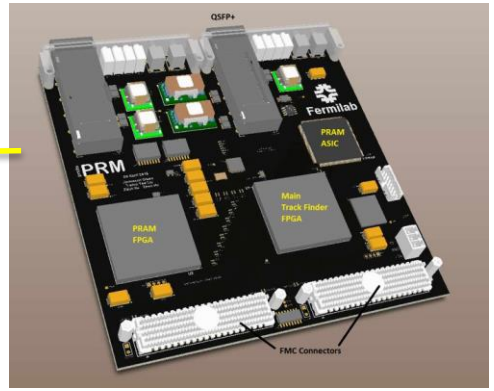
Initial System Demonstration



Select 40 modules







Data Source:
Emulating ~40 modules

Δt1 (Data Delivery) + Δt2 (PR) + Δt3 (TF)

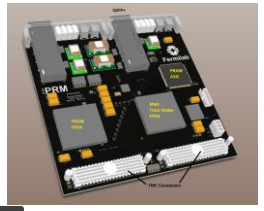
Stages of the Demonstration System

Data Sourcing

Emulate data coming from the detector.

Data Delivery

Deliver stubs to the pattern recognition engine.



Pattern Recognition

Fast PR using bank of AM chip.

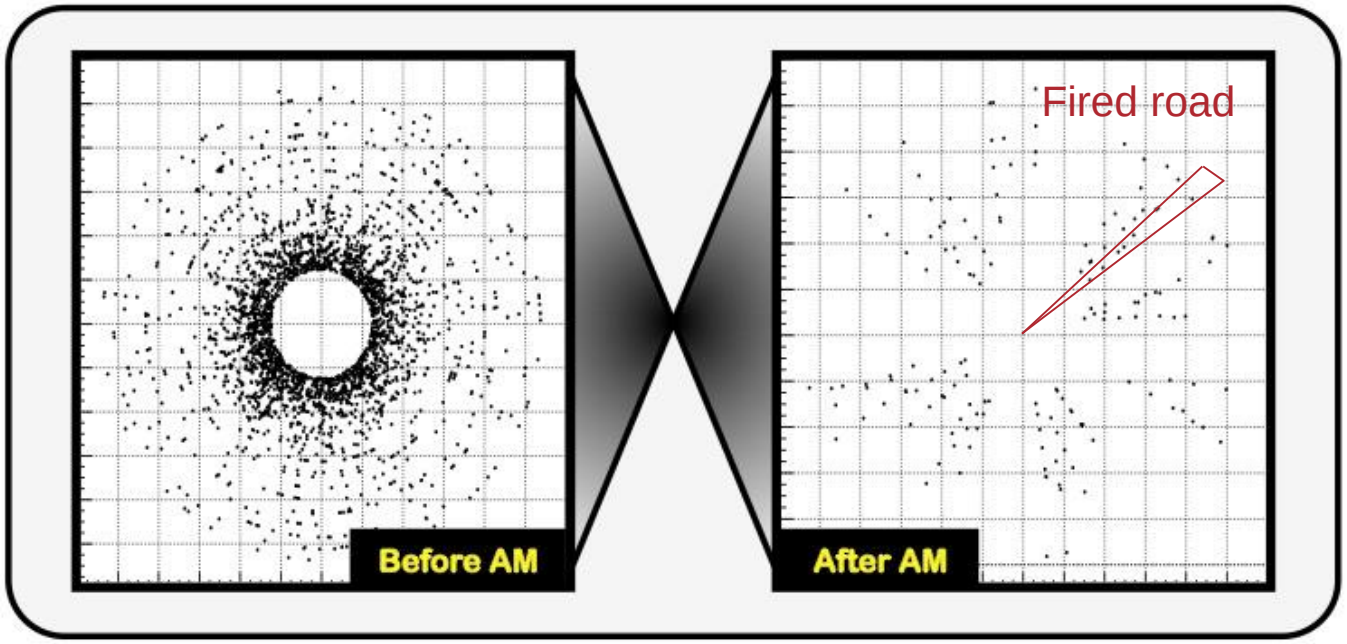
Track fit

Calculate track parameters in FPGA.

Data Sourcing and Delivery

- Preparing simulated data (MC events), software and firmware (access to the board, FPGA data communication) for Data Sourcing.
- For the Data Delivery, preparing Pattern Recognition Board Firmware for the data formatting.
- 2016: Full demonstration with two crates.

Pattern Recognition + Track Fitting

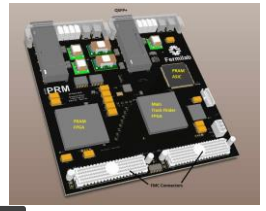


- Identify consistent hits in the detector for a potential track, checking the AM bank.
- Calculate track parameters on FPGA

Stages of the Demonstration System

Data Sourcing

Data Delivery



Pattern Recognition

Track fit

Emulate data coming from the detector.

Deliver stubs to the pattern recognition engine.

Check patterns in AM chip.

Calculate track parameters in FPGA.

Make sure that the optic fiber communication between boards is robust!

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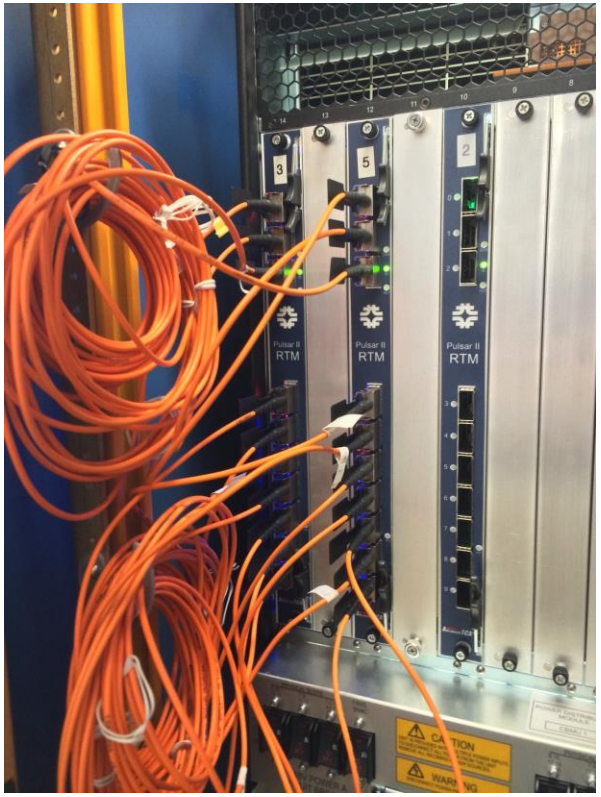
Pulsar IIb link performance



- Installed Link Test Firmware (that uses PRBS test pattern generation) on two boards.
- Connected pairs of ports (8 links per pair) on the RTMs.

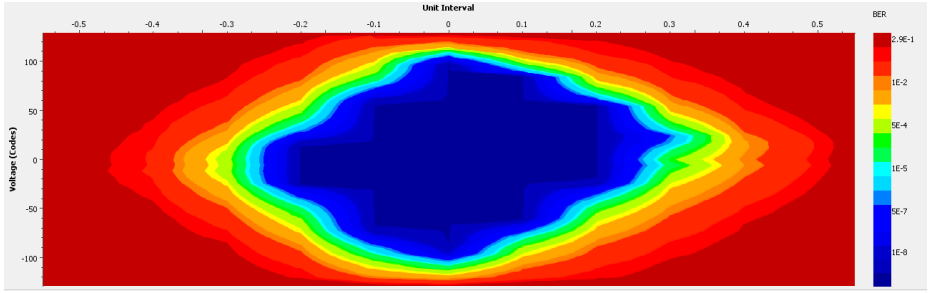
At high data transfer rates many factors influence link performance:

- Crosstalk.
- Attenuation.
- Impedance mismatch.
- Reflections.

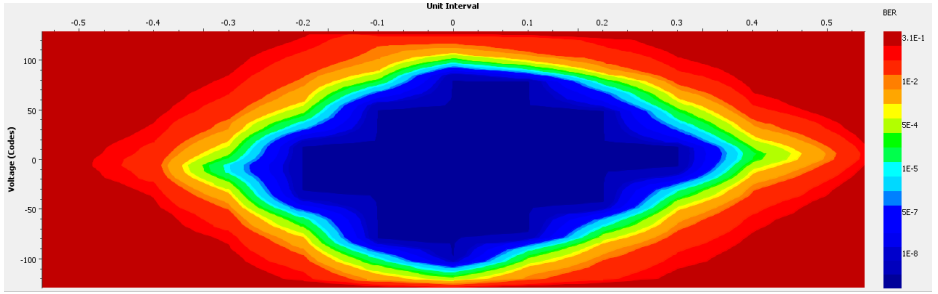
Pulsar IIb link performance

Studied different scenarios:

- Link setups.
- Molex and 3M optic fiber cables.
- Speed rates, signal parameters.



Used the Vivado Serial Link Analyzer Tool to apply link settings and parameters, and to generate statistical eye diagrams (right).



- Time (horizontal) and voltage (vertical) offset values for the data samples sent.
- The colors represent a logarithmic scale for the Bit Error Ratio.

Pulsar IIb link performance

Tunes:

- Signal amplitude (866 mV).
- Pre-cursor and post-cursor emphases.
- One directional (required) vs bi-directional communication.

The size of the area with the smallest error rate (blue) is a measure of the tolerance of the system to offset values on the data.

Each channel (@ 10Gbps, 3M cable) is stable and has been tested at Bit Error Ratios down to 10^{-14}.

Summary

- HL-LHC = high data volume (100 Tbps) and short latency (few μs) required for the new Tracking Trigger system at CMS.
- A demonstration of the system is currently being prepared at FNAL.
- Importance of the robustness of the high-speed communication between data sourcing and PRBs.
- Using the Link Test firmware and generating the eye diagrams, several link configurations have been studied.
- For the configuration to be used in the demonstration, each link is stable at 10 Gbps and has been tested at Bit Error Ratios down to 10^{-14}. This hardware performance is good for the demonstration.

My experience

- My first time working on digital electronics.
- Big collaboration (~100 people) - many countries and institutions.
- Thanks to Zijun, Ted, Jamieson and Zhen for letting me “play” with very (very!) hi tech hardware, and for all the help.